Advantest R3132 Local oscillator 3840MHz (2e Mixer) problem

Problem:

The spectrum analyzer works fine for a couple of minutes after cold start but the measured level slowly fades and after a couple of minutes of warming up the frequency drifts and becomes unstable.

This fine instrument is terrible to repair, it is almost impossible to perform measurements inside the unit while it is operating and a service manual cannot be found (frustration of many users I guess). The article from Mr. Fraser Castle (10 feb 2013) helped me on the way of starting a repair attempt.

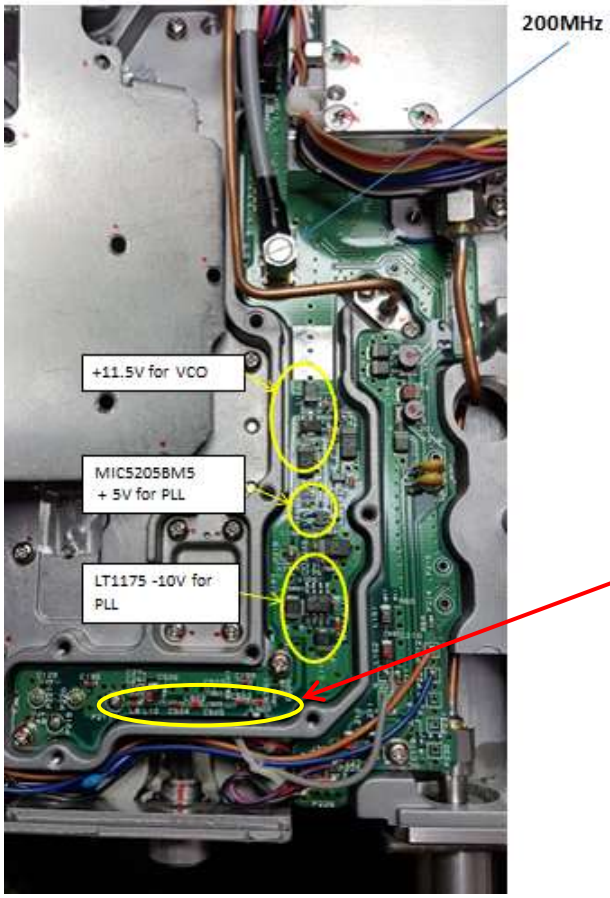
My first guess was that the oscillator had a thermal problem and drifted outside the lock range. Re-adjusting the oscillator as explained by Fraser however did not solved the problem.

My second guess was that the PLL circuit had problems. Everything I found about this PLL circuit was not usable. I only have sporadic access to a spectrum analyzer that measures above 3GHz so I had to be inventive to do some measurements in the circuit with what I have at home. I wanted to measure inside the PLL but then I first have to understand how the circuit worked.

It was a lot of work but I managed to do a complete reverse engineering (under a microscope) of this circuit and was able to drawn the circuit. The operation of this PLL is quit clever and contained some circuit surprises.

Figure 1 Microscope examination (reverse engineering at work ☺)

I walk you through my quest with some pictures, don't worry the actual circuit can be found further on.

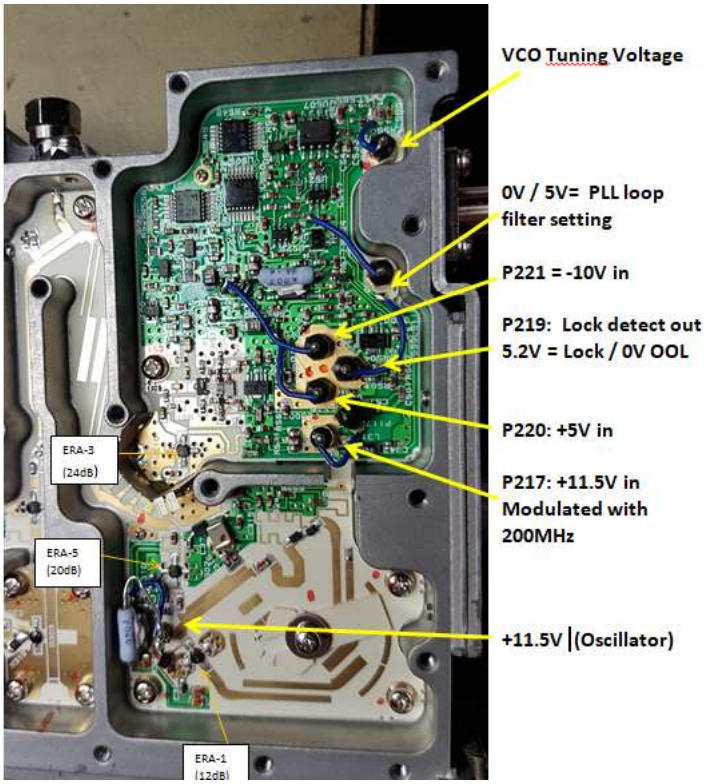


When you remove the controller board and the metal cover plate on the back of the PLL You will find the local power supplies for the VCO and the PLL and also the coaxial cable that delivers a 200MHz reference clock for the PLL.

Note that the local power supply can be switched on and off by software.

The power is fed to the PLL on feedthrough capacitors. The 200MHz reference frequency is capacitive coupled on the +11.5V by a filter network. *Not expecting this one!*

Figure 2: TOP side of PLL with feedthrough caps, and local power supplies



The complete PLL circuit is in this box. Only the power and 200MHz reference frequency are needed. The VCO tuning voltage feedtrough is an output that is routed back to the controller board, probably for monitoring.

Figure 3: Open PLL and Oscillator

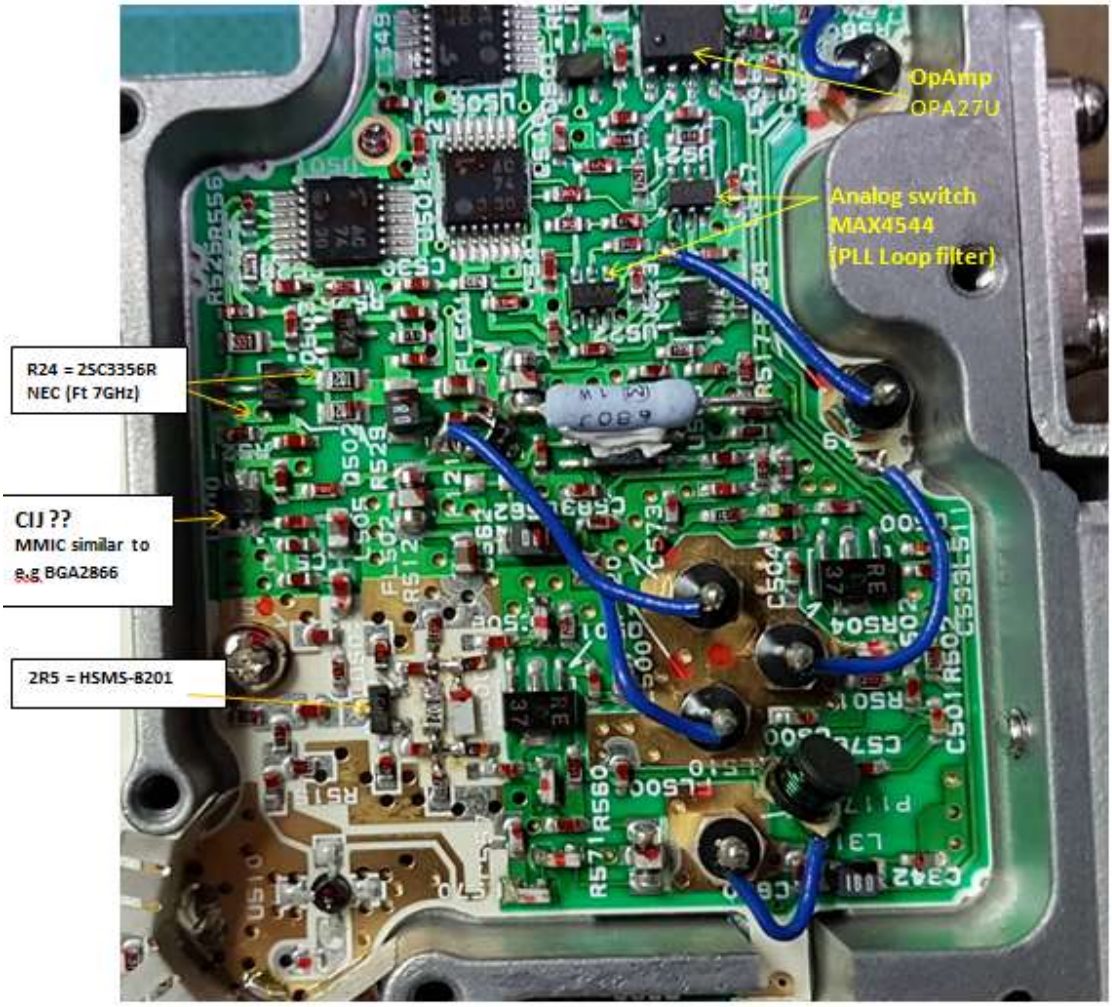


Figure 4: Close-up PLL

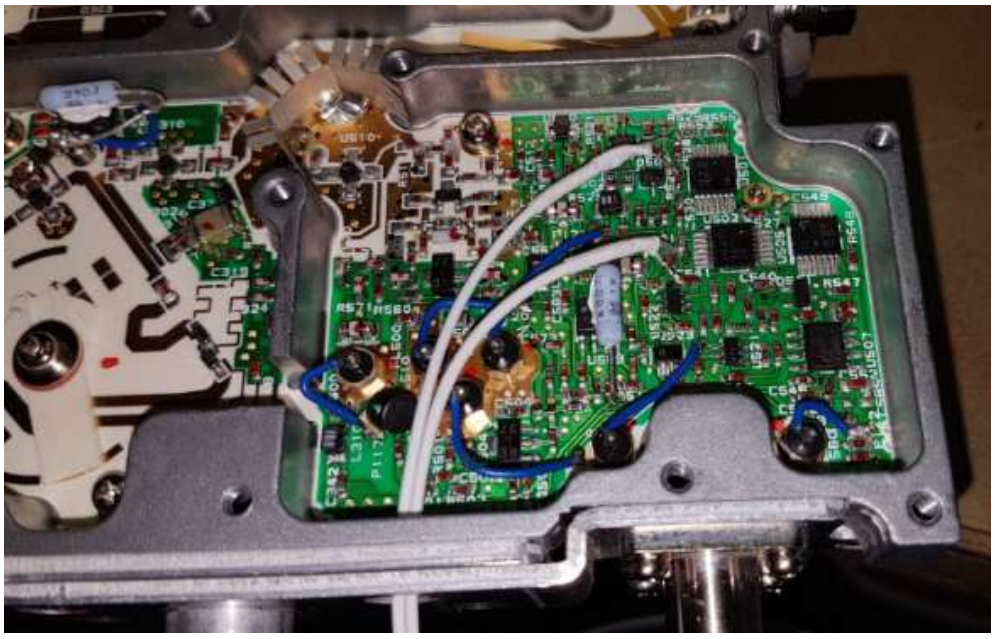


Figure 5: Measurement of phase detector input using thin coax (40Mhz top, 20MHz reference bottom)

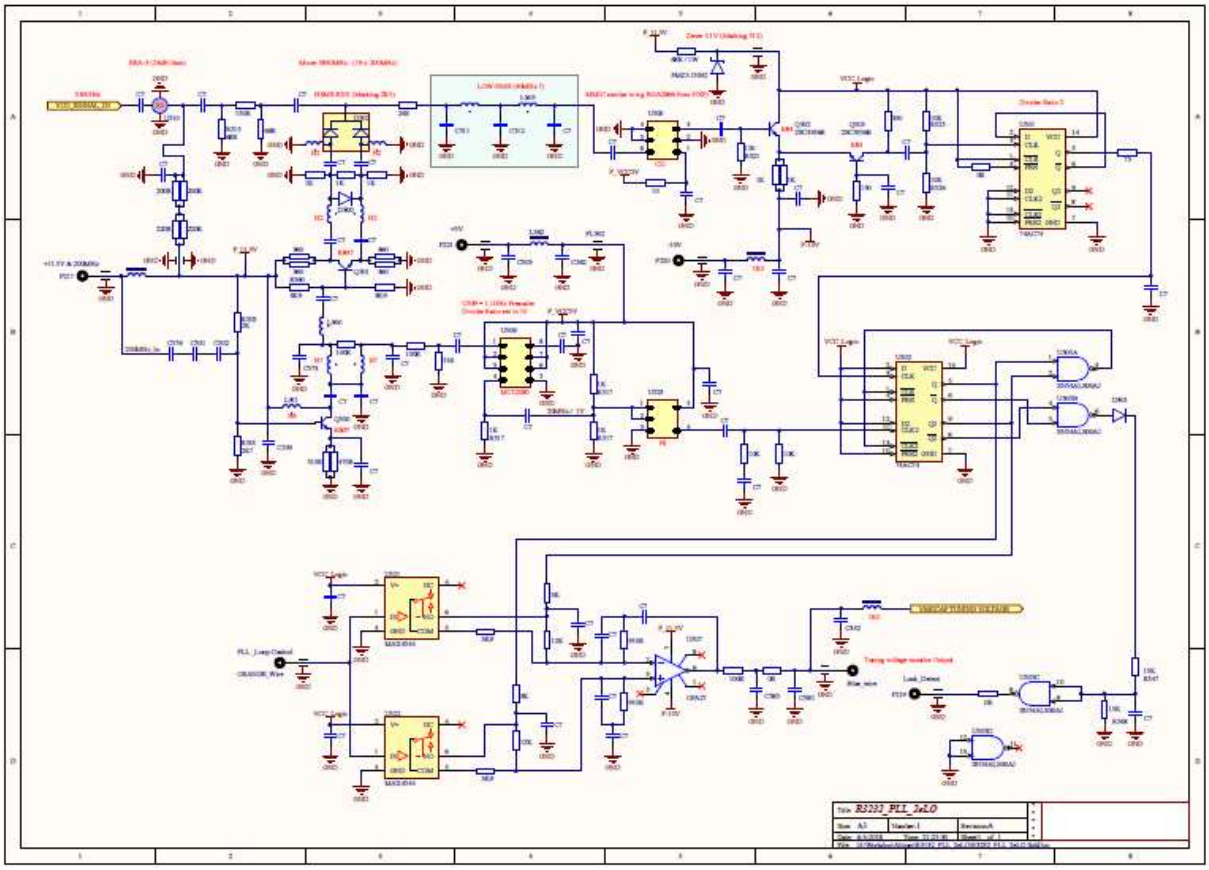


Figure 6: Reversed engineered circuit of the PLL

The circuit:

The 200MHz clock signal is extracted from the power supply and amplified by Q500. The output is fed to a PECL divider U509 and divided by 10 to generating a 20MHz reference for the PLL. The 200Mhz is also amplified and send to an harmonic generator Q501 and D500.

The VCO signal is amplified by an ERA-3 MMIC and mixed with the harmonics by D501. The 19e harmonic of 200MHz is 3800Mhz, the difference is 40Mhz.

The output of the mixer is send through a 40MHz Low-pass and amplified by U500. (U500 is an unknown MMIC that could possibly be replaced by a device from the BGA286x family of NXP.)

The amplified 40Mhz signal is divided by 2 by U501 (74AC74 flip-flop).

A second flipf-flop (U502) and the 2-input NAND-gate U505A forming the phase comparator. The outputs are connected to the Op-Amp OPA27. The output of this integrator / filter is fed to the varicap diodes of the VCO.

The loop time constant of the PLL can be changed by opening or closing the analog switches U521 – U522.

A Lock-Detect output is made with D501, an RC network and U505B and U505C

Nice ☺

I added all component values and designators that I could identify. The capacitor values are unknown but not important to understand the working of the circuit. Some of the SMD markings are unknown to me (I could not find anything on the net). Help is welcome here to complete the circuit even further.

***Note:** When the VCO is mistuned then it could lock to a different harmonic of 200Mhz, e.g. the 18e or 20e . This might result in a stable locked VCO but at a wrong frequency. I remember someone struggling with this problem.*

Tracing the problem:

Now that I knew where to measure I stared with comparing the two clock signals for the PLL (Figure 5) And I noticed that the amplitude of the down mixed VCO signal fades away into the noise after a couple of minutes and it takes up to an hour or so of power-down before it resumes operation.

I then decided to measure the output signal of the oscillator on the SMA test connector. I don't have a spectrum analyzer for this but I do have a calibrated Power meter up to 18 GHz.

Problem is that you cannot connect a SMA connector and insert the module because the connector is sticking out. I decided to make a direct coax connection on the inside of the unit and measure the output level during warm-up.

I removed one of the screws of the SMA plug and pulled the coax shield in the hole. I wedged it with the tip of a tooth stick (pls don't laugh).

I fixated the cable to the frame at several places an lead it to the back of the unit.

Figure 7: Coax entering the unit

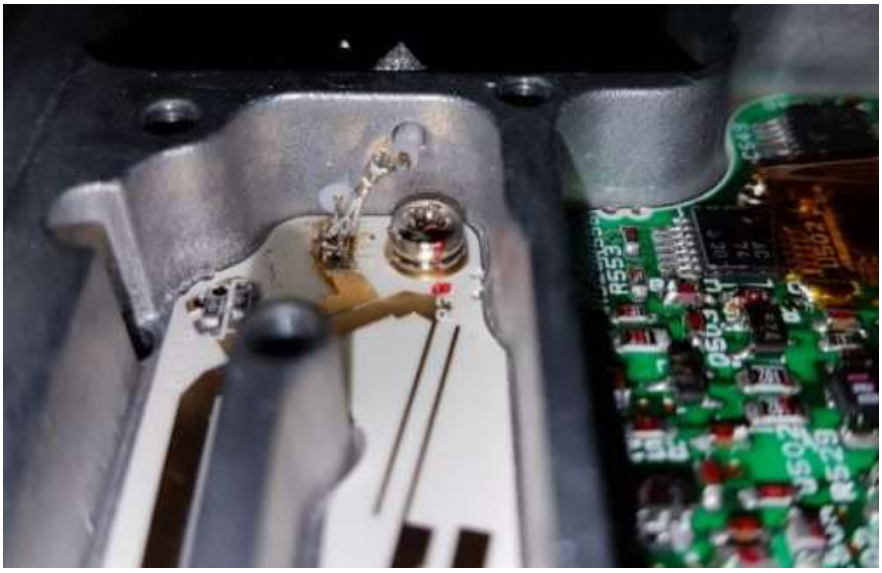


Figure 8: Coax soldered to the stripline

I connected the CAL OUT signal to the RF input and monitored the oscillator level and Calibration level during warm-up

Time minutes	dBm@3.84GHz	dBm measured @ 30MHz	PLL Lock
0	-26,81	-21,19	OK
1	-27,66	-21,32	OK
2	-28,35	-21,59	OK
3	-29,47	-21,7	OK
4	-30,74	-22,6	OK
5	-33,26	-24,4	OK
6	-36	-52	OOL
7	-47,2	-76	OOL

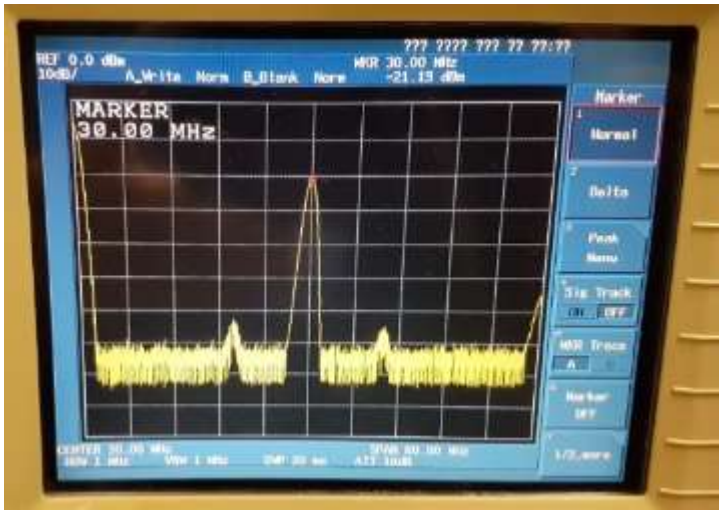


Figure 9: CAL value at cold start

Figure 10: 3.84GHz output cold start (note that this is almost 10dB lower then what other guys have measured)

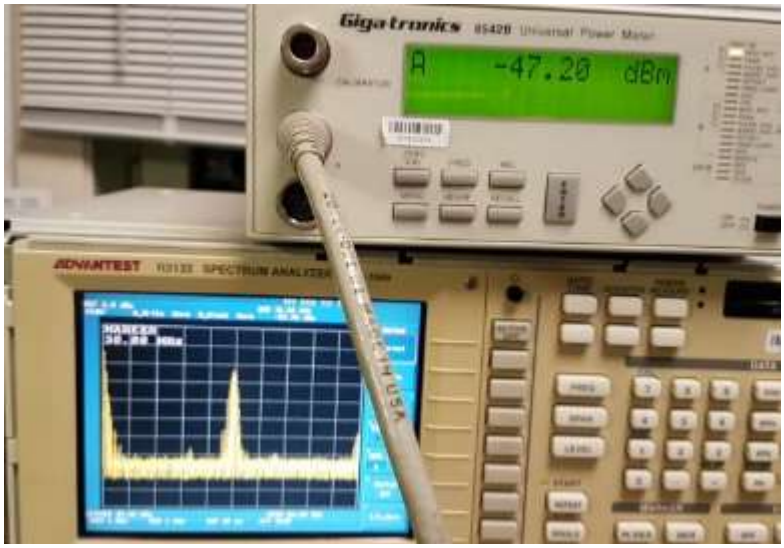


Figure 11: measurements after 7min On

Conclusion of the Quest:

After these measurements it was clear that the VCO output level having thermal issues . My money is on the buffer MMIC (ERA-5) as culprit. I have ordered some devices now to replace the MMIC's in the VCO (I found the MMIC's here www.funkamateur.de).

At the end of the day, it looks as my reverse engineering job was not required but then it could be beneficial for a lot of other enthusiast.

I try to keep you posted on the final results of the repairs.

73 to all Ham's